CLAIMS

What is claimed is:

1. A variable gain amplifying stage in a transmitter chip, said variable gain amplifying stage comprising:

a first circuit operable to provide a current drive signal in response to a reception of a voltage control signal and voltage intermediate frequency signal by said variable gain amplifying stage, said current drive signal having an AC current component and a DC current component;

a second circuit operable to provide a DC current control signal in response to a reception of said voltage control signal by said variable gain amplifying stage; and

wherein a ratio of a first ampere level of said DC current component of said current drive signal to a second ampere level of said DC current control signal is constant.

2. The variable gain amplifying stage of claim 1, wherein

said second circuit is a replica of said first circuit.

3. The variable gain amplifying stage of claim 1, wherein

means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a voltage level of said voltage control signal.

4. The variable gain amplifying stage of claim 1, wherein

means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a temperature of the transmitter chip.

5. The variable gain amplifying stage of claim 1, wherein

means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a processing performance of the transmitter chip.

6. The variable gain amplifying stage of claim 1, wherein

means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a supply power of said transmitter chip.

7. A transmitter chip, comprising:

a variable gain amplifying stage operable to provide a current drive signal and a DC current control signal, said DC current drive signal having an AC current component and a DC current component;

a biasing stage operable to provide a first DC current biasing signal in response to a reception of said DC current control signal; and

wherein a first ratio of a first ampere level of said DC current component of said current drive signal to a second ampere level of said DC current control signal is constant.

8. The transmitter chip of claim 7, wherein

said variable gain amplifying stage includes means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a voltage level of said voltage control signal.

9. The transmitter chip of claim 7, wherein

said variable gain amplifying stage includes means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a temperature of the transmitter chip.

10. The transmitter chip of claim 7, wherein

said variable gain amplifying stage includes means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a processing performance of the transmitter chip.

11. The transmitter chip of claim 7, wherein

said variable gain amplifying stage includes means for adjusting said ampere level of said DC current component of said current drive signal and said ampere level of said DC current control signal in response to any variation in a supply power of said transmitter chip.

12. The transmitter chip of claim 7, wherein

a second ratio of said second ampere level of said DC current control signal to a third ampere level of said first DC biasing current signal is constant.

13. The transmitter chip of claim 7, further comprising:

a phase shifting stage operable to provide a current intermediate frequency signal in response to a reception of said DC current drive signal and said first DC biasing current signal.

14. The transmitter chip of claim 13, further comprising:

a mixing stage;

wherein said biasing stage is further operable to provide a second DC biasing signal in response to a reception of said DC current control signal; and

wherein said mixing stage is operable to provide a current radio frequency signal in response to a reception of said current intermediate frequency signal and said second DC current biasing signal.

15. The transmitter chip of claim 4, wherein

a second ratio of said second ampere level of said DC current control signal to a third ampere level of said second DC biasing current signal is constant.

16. The transmitter chip of claim 14, wherein

a gain of said mixing stage is constant.

17. A transmitter chip, comprising:

a mixing stage; and

means for operating in a current mode of operation to establish a constant gain of said mixing stage.

18. A method for dynamically biasing a transmitter chip, said method comprising:

generating a current drive signal in response to a reception of a voltage control signal and a voltage intermediate frequency signal, said current drive signal having an AC current component and a DC current component; and

generating a DC current control signal in response to a reception of said voltage control signal,

wherein a first ratio of a first ampere level of said DC component of said DC current drive signal to a second ampere level of said DC current control signal is constant.

19. The method of claim 18, further comprising:

generating a first DC current biasing signal in response to a generation of said DC current control signal,

where a second ratio of said second ampere level of said DC current control signal to a third ampere level of said DC current biasing signal is constant.

20. The method of claim 19, further comprising:

generating a current intermediate frequency signal in response to a generation of said fist DC current drive signal;

generating a second DC current biasing signal in response to a generation of said DC current control signal; and

generating a current radio frequency signal in response to a generation of said current intermediate frequency signal said and said second DC current biasing signal.